Bidirectional power supply documentation

Release 0.1

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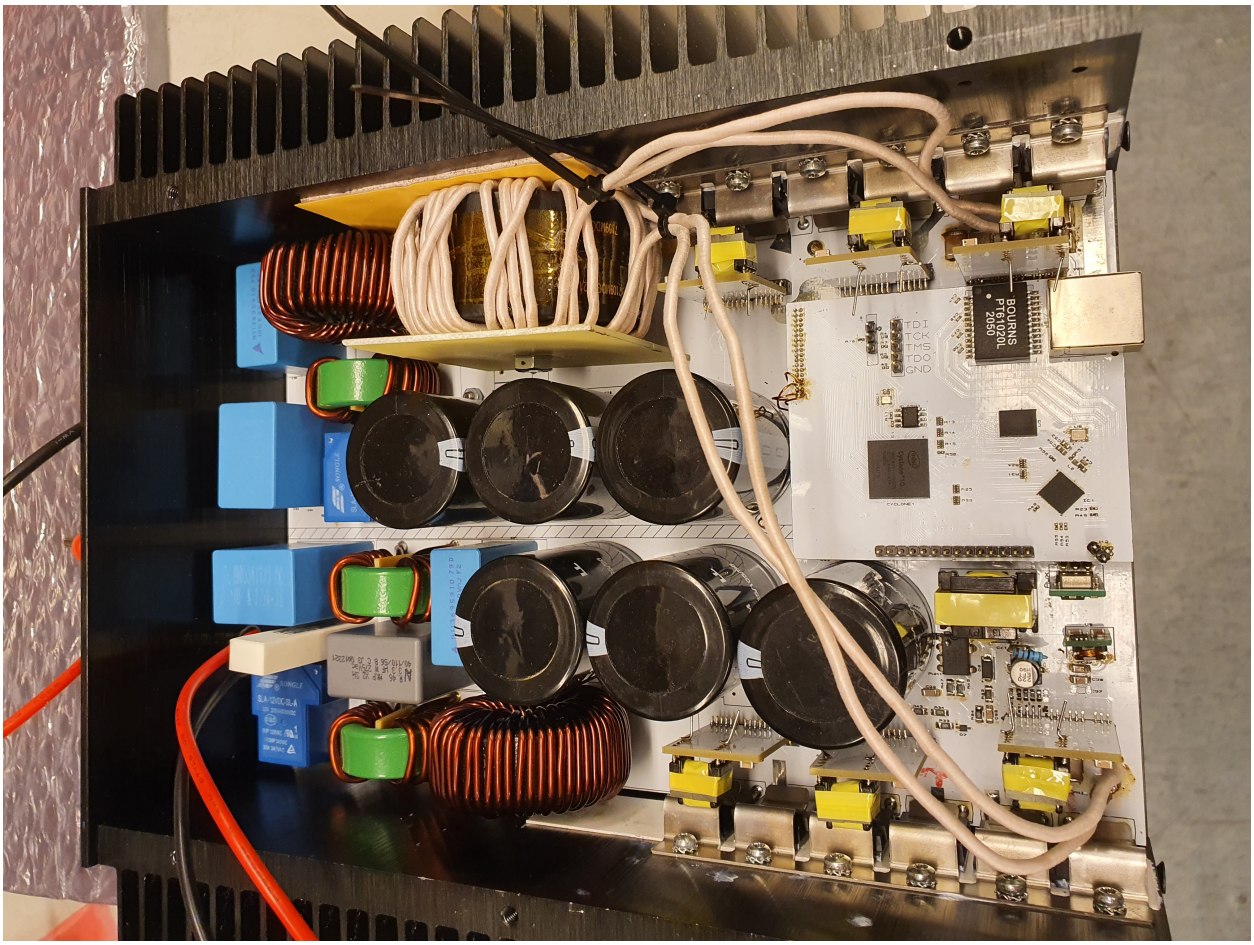
Sep 13, 2022

ABOUT



These are documentation pages and build log for fully FPGA controlled bidirectional power supply. The code can be found in github at

https://github.com/johonkanen/ac_in_ac_out_lab_power_supply

The VHDL code for this project is built using hVHDL libraries. The hVHDL libraries and high level methods allow the code to be written at high level and the methods allow for very fast development and continuously improvement and reuse of existing code. The hVHDL project is open source and can be found in Github

https://github.com/hVHDL

I have written about the design methods and some of the math behind this power supply at my home page https://hardwaredescriptions.com

I have opened a discussions page in the github where you can write any comments, questions or general ideas. If there is some other platform better suited for this you can write a comment in the discussions page. https://github.com/johonkanen/ac_inout_power_supply_docs/discussions

The pcb files are found on the documentation github page at https://github.com/johonkanen/ac_inout_power_supply_docs/tree/main/pcb_files

The pcbs are designed using Proteus Professional, which has a fully featured demo version with which you can view the schematics. The demo version can be downloaded for free at https://www.labcenter.com/downloads/

CHAPTER

ONE

CONTINUOUS INTEGRATION FOR VHDL

The project is developed using the idea of continuous integration. This means that the code is continuously build with the target device and developed in small increments. The main branch is kept in functioning shape at all times and the code is run against tests.

1.1 Managing dependencies with test driven development

I strive for using tests that the development is run against. The project is developed 90% using a test framework called VUnit. This allows evaluating all tests all the time, which keeps the tests in operating state. Making tests, even completely superfluous ones has a great advantage. They keep individual pieces of code individual. Since there is only minimal amount of code build for each test, the dependencies, that is the number of source files needed for using a piece of code is kept to a minimum.

The individual modules are also developed in separate repositories. This allows a minimal number of sources to be reused for many different projects. It also helps to keep the interdependencies to a minimum. It is very difficult to add sources from separate repositories to new ones, thus this helps keeping separate things separate.

I have written about code structures in VHDL that allow for managing dependencies with the language features of VHDL at https://hardwaredescriptions.com/dependency-management/

CHAPTER

TWO

WHAT IS THIS PROJECT?

This project is a bidirectional lab power supply. The idea is to have a programmable supply with which I can relatively easily develop grid connected devices, or other power supplies. The bidirectionality allows the power supply to work as either a load or a source.

The power supply is designed with a grid side inverter and a load side inverter and these are galvanically isolated with a dual active bridge DC/DC converter.

The converter is controlled using a FPGA. The use of an FPGA greatly simplifies the hardware design, since we can use any adcs for measurements and control and we can effectively route the digital lines in the programmable chip it self, thus we can select IO:s based on what is simple to route. Also the gate power supplies can be controlled with the FPGA.

CHAPTER

THREE

SIMULATIONS AND TESTS FOR IO

The most difficult part of any embedded system is the interfacing from the code to outside world. This requires understanding the documentation and using different interfaces and peripherals exactly according to the intended way. The difficulty is that there is rarely a possiblity for simulating the used configuration unless test driving it with the actual hardware.

With FPGA IO are developed exactly the same way as any other modules. We can use simulations and tests just as with any other modules. This allows us to run the same code in a simulation that we run in the actual hardware.

CHAPTER

FOUR

AUXILIARY SUPPLIES

The power supply is designed to be operated from the line voltage, but the measurements and control and logic circuits need various different voltages to functino correctly. These low power lines are the auxiliary voltages we need to design. The power supply of choise for isolating the primary and secondary side control voltages from the high voltage DC link is discontinuous mode flyback power supply. The flyback requires a minimum amount of parts, since only a transformer, controller and a diode and a capacitor is required and any extra voltage requires just an additional winding to the transformer and a diode + capacitor.

The voltages that are needed by the circuits are 15V for the isolated voltage, +15/-4 for each switch gate, 5V for sigma delta adc:s and the regulated intermediate voltage and then 3.3, 2.5 and 1.2 for the FPGA, 3.3V for the measurement circuits and 1.75 for the op amp references.

The regulated 5V supply line is obtained from an non-isolated switching regulator. The lower voltage 3.3V is otained from the 5V with a linear regulator.

The 5V could also be an additional secondary from the flyback. For first iteration of the power supply card, the extra fiddling of the getting the 5V secondaries to behave correctly is prevented by using a regulator. The primary and secondary sides have own supplies thus instead of 2 semi well regulated secondaries, we would need 4 semi regulated secondaries. In my experience this would require a day or two of extra testing and iteration with the flyback transformer.

4.1 DCM flyback design

Since dcm flyback is very common, there are a complete solutions available that does everything using just a single chip. The simplest chip for this that I have come accross is the family of of primary side feedback flyback controllers from Dialog Semiconductor. For this application, I chose IW1818 which allows for approximately a 10W flyback to be built. The IW1818 is a quasi resonant controller and the magic lies in that the feedback is taken from the primary side switched node. The measurement is taken from the reflected voltage of the transformer and this actually is influenced by all secondary voltages. Hence the feedback is taken automatically from all windings.

The IW1818 has very good cross regulation. This was tested in a lab with 200mW and 5W loads at which the primary and secondary were measured between 15.3V and 14.6V with 15 V being the design goal.

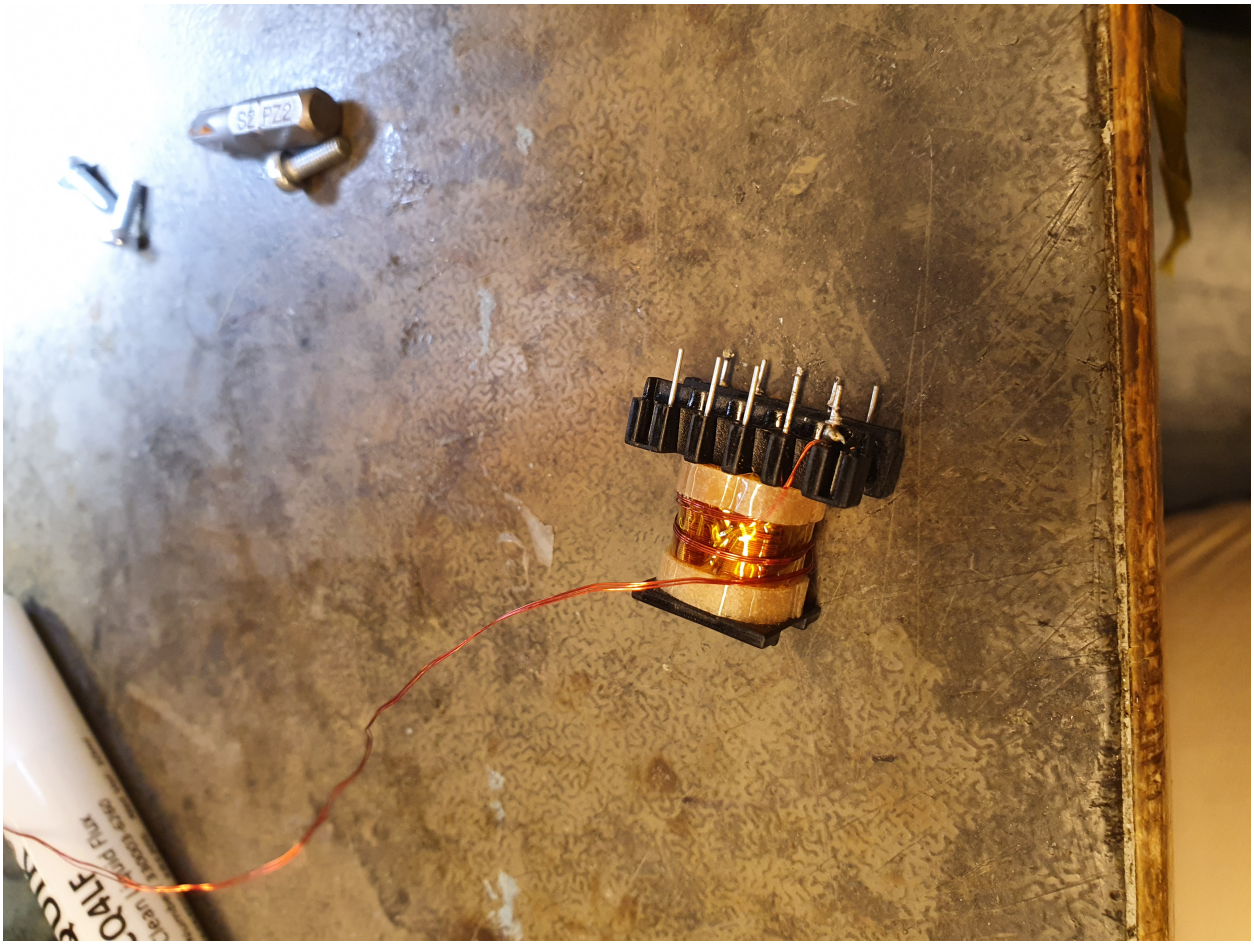
4.2 Transformer design

The transformer design for low power DCM flyback is relatively simple. The transformer design is just copied from Fairchild Application Note AN4137.

The design is very simple, just add desired core cross-sectional area and then iterate powers, voltages and the ripple factor to obtain a reasonable design where the windings are close enough for full turns. The design that I used has 52 turn primary, 8 turn secondaries and an off the shelf 250um gapped ee20 core of ef87 ferrite material. The coil formers and border tape are from aliexpress.

The flyback cross regulation is greatly impacted by the winding layout, thus some iteration will be necessary to get it right. In this case the used wires and winding layout was deemed good enough with only a few tests.

The structure of the used transformer is visible in the picture talen during winding. There are 3mm border tapes on both sides of the transformer and the windings are built from 3 strands of awg34 wire and all windings are isolated with 3 layers of capton between them. The wires are not twisted together since the transformer is easier to wind in this way. Note that the ends are not sleeved even though this would be required for off line transformer thus new transformer needs to be built with the ends pulled out of the winding inside proper extra isolation.



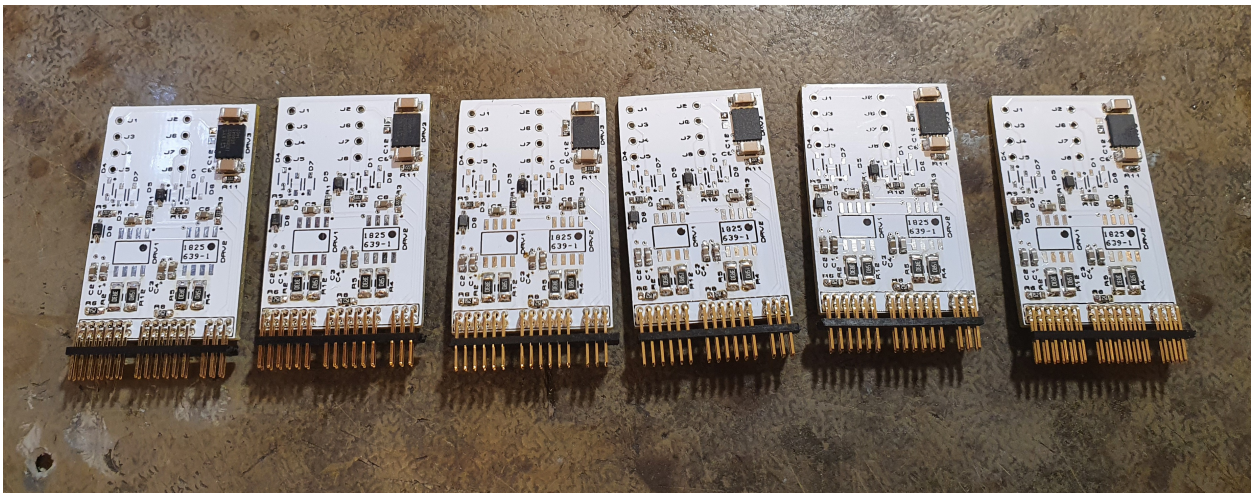
CHAPTER

FIVE

GATE DRIVE POWER SUPPLY

The gate drivers also need to have a distinct power supplies. The main design goal of a gate drive power is that it is simple and small and provides voltages for the SiC gates. The accuracy for this does not need to be perfect, so anything between 14.5 and 16 V should be sufficient at this point. I have designed two versions of the gate drive power supply. One is build using a asymmetric flyback and the other is just basic flyback with a single transistor and rcd snubber. The gate drive power is operated open loop thus it is important that the supply has good open loop regulation. In my experience, the asymmetric flyback does this well enough. I have used an ixys IXDD609 gate driver as the power stage to drive the transformer. Since the secondaries are the same for both, the flyback and asymmetric flyback, I also ordered boards for the flyback.

The partially assembled boards are visible in the Figure below.



The gate power supplies have an EE10 transformers for each board and every board creates voltages for one half bridge. Additionally one of the pins is just the raw 15V voltage, which is used for powering the isolated ADC that is used to measure the inductor currents.

5.1 Gate power transformer design

The transformer has 5 windings. 8 turn primary with 4 and 14 turn secondaries for the 15V and -4V voltages. The transformer design is pretty much based on just having a good enough unregulated voltages. From experience I know that a 8 turn primary will be sufficient to prevent in this configuration excessive core loss. However since the regulation of the voltages is dependent on the diodes, stray inductance and input voltages, all of which have some uncertainty the design is more or less trial and error with the hardware. I found that a satisfactory design was with primary wound as the first layer and then the secondaries are wound in two separate sections such that for one winding the 4 and 14 turn

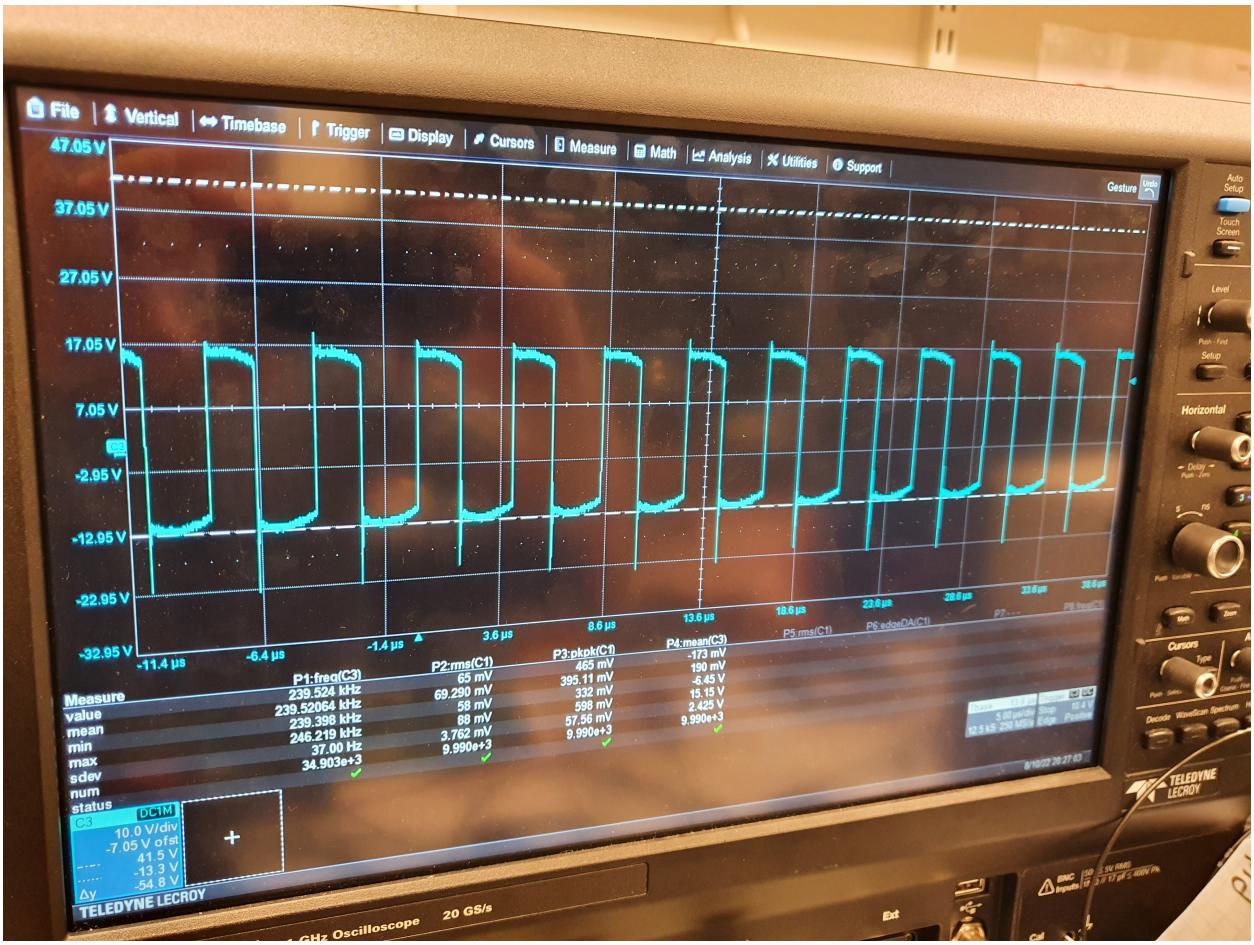
secondaries are on top of each other. This way the winding is quite symmetric and that should result in good enough cross regulation. The increased stray inductance also is useful for reducing inrush current.

The transformer before final taping is shown below. The two pairs of secondaries are wound in similar fashion side by side and a layer of tape is placed between them

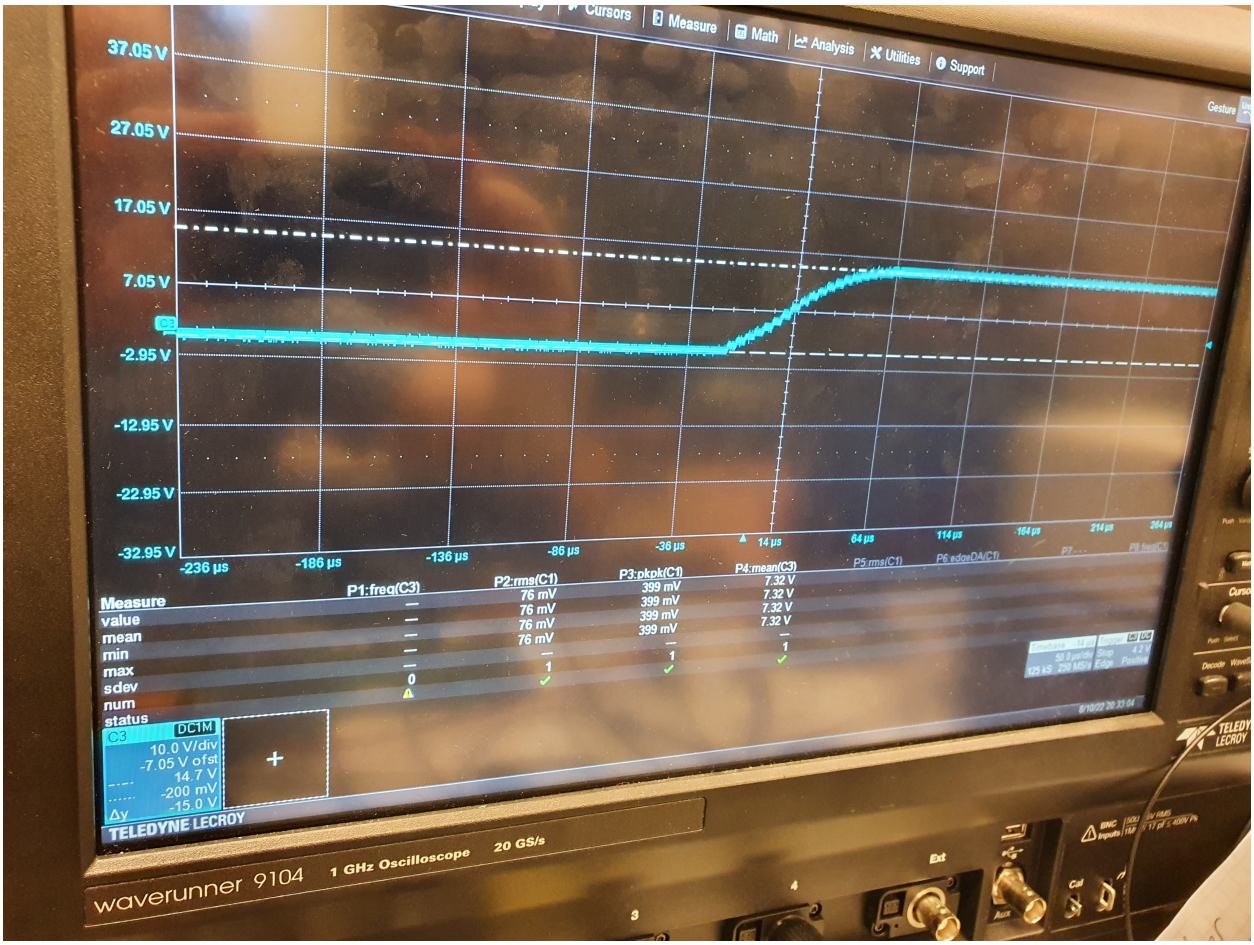
5.2 Gate power measurements

The gate power supply has no snubbers, but due to the losses in the gate drive transformer it self the the achieved waveforms are fairly clean. The -4V bias for the gates show almost perfect square voltage waveforms and the 15V high voltage winding shows manageable undershoot with very little ringing.


Vertical
Timebase
Trigger
Display
Cursors
Measure
Math
Analysis
Utilities
Support
47.05 V
37.05 V
27.05 V
17.05 V
7.05 V
-2.95 V
-12.95 V
-22.95 V
-32.95 V
-11.4 µs
-6.4 µs
-1.4 µs
3.6 µs
8.6 µs
13.6 µs
18.6 µs
23.6 µs
28.6 µs
33.6 µs
38.6 µs
P5:rms(C1)
P6:edgeDA(C1)
Measure
value
mean
min
max
sdev
num
status
P1:freq(C3)
239.570 kHz
239.52018 kHz
239.472 kHz
239.586 kHz
21.35 Hz
13.387e+3
P2:rms(C1)
71 mV
71.451 mV
62 mV
85 mV
3.587 mV
1.217e+3
P3:pkpk(C1)
399 mV
371.72 mV
332 mV
465 mV
38.78 mV
1.217e+3
P4:mean(C3)
-136 mV
-143.67 mV
-177 mV
-110 mV
10.23 mV
1.217e+3
DC1M
10.0 V/div
-7.05 V ofst
41.5 V
-13.3 V
-54.8 V
Δy
TELEDYNE LECROY
waverunner 9104
1 GHz Oscilloscope
20 GS/s
Gesture
Horizontal
Cursors
Ext
Aux
Cal
TELEDYNE LECROY



There is no rampup of the pwm waveforms, thus the stray inductance and circuit resistances are what restrict the gate power supply current during transient. Since there is no DC inductor, the gate power natural rampup is very clean with no overshoot.



5.3 Notes

The first implementation of the gate drive powers is quite lossy. Powering all 12 gates of the power supply takes roughly 4.5 W which seems a bit high, but there is no thermal issues and I let it run for several hours, so it seems to work well enough for now.

CHAPTER

SIX

FPGA CONTROL CARD

The system is controlled using a Cyclone 10 LP FPGA. The control card is placed in the secondary side of the power supply. The control card has connections for a serial connection, gigabit ethernet for the main communications, a single row header that can be used for a LCD display and the 5V and main connectors between control card and the power card. The power card has primary side measurements and the underside of the control card has the secondary measurements. All currents are measured using isolated sigma delta modulators as these can be operated from the gate drive power supplies and can be directly interfaced to a shunt resistor. The use of a resistor in place of a dedicated current transducer is much simpler, cheaper and require a lot less board space.

Interestingly the first revision of the power supply board has a bug in that the main connector is mirrored. However, since an FPGA is used here, the fix is simply to reroute the IO:s in the build script and swap 4 pins due to opposing ground connection.

6.1 ADS7056 AD converter

The ad converter that is used on the control card are texas instruments ADS7056 type. These are SAR adc with internal sample and hold circuitry and it allows up to 2.5 MHz sample rate. The ADC is controlled with SPI, which makes it simple to operate. The sample ADC is used for sampling multiple signals, hence an analog multiplexer is used to switch between the adc inputs.

6.2 Ethernet PHY

The ethernet chip is PEF707 as this is the same as is used with the cyclone 10 lp evaluation kit. The Ethernet phy has an onboard switched mode controller that makes powering the phy very simple.